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| Applicant | : Shunpei Yamazaki et al | Art Unit | : 2891 |
| Serial No. | : 09/894,950 | Examiner | : Caridad Everhart |
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| Title | : SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF | | |

**Mail Stop Amendment**
Commissioner for Patents
P.O. Box 1450
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**AMENDMENT IN REPLY TO ACTION OF OCTOBER 12, 2005**

Please amend the above-identified application as follows:

**Amendments to the Claims** are reflected in the listing of claims which begins on page 2 of this paper.

**Remarks/Arguments** begin on page 14 of this paper.

Amendments to the Claims

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims

1. (Currently Amended) A semiconductor device comprising:

a shielding film and a gate signal line formed on an insulating surface;

a planarization insulating film formed so as to cover the shielding film and the gate signal line; and

a semiconductor layer having a channel formation region formed over the planarization insulating film,

wherein the shielding film overlaps the semiconductor layer with the planarization insulating film sandwiched therebetween~~, and~~

~~wherein the planarization insulating film is polished before the semiconductor layer is formed~~.

2. (Previously Presented) A device according to claim 1, wherein thicknesses of the shielding film and the gate signal line are 0.1 $\mu$m to 0.5 $\mu$m.

3. (Currently Amended) A device according to claim 1, wherein the shielding film and the gate signal line are tapered ~~around the edge~~.

4. (Original) A digital camera comprising a semiconductor device according to claim 1.

5. (Original) A video camera comprising a semiconductor device according to claim 1.

6. (Original) A goggle type display device comprising a semiconductor device according to claim 1.

7. (Original) An audio system comprising a semiconductor device according to claim 1.

8. (Original) A notebook personal computer comprising a semiconductor device according to claim 1.

9. (Original) A portable information terminal comprising a semiconductor device according to claim 1.

10. (Original) A DVD player comprising a semiconductor device according to claim 1.

11. (Currently Amended) A semiconductor device comprising:

a shielding film and a gate signal line formed on an insulating surface;

a planarization insulating film formed so as to cover the shielding film and the gate signal line; and

a thin film transistor including an active layer, the transistor being formed over the planarization insulating film,

wherein the active layer has a channel formation region, and

wherein the shielding film overlaps the channel formation region with the planarization insulating film sandwiched therebetween~~, and~~

~~wherein the planarization insulating film is polished before the active layer is formed~~.

12. (Previously Presented) A device according to claim 11, wherein thicknesses of the shielding film and the gate signal line are 0.1 $\mu$m to 0.5 $\mu$m.

13. (Currently Amended) A device according to claim 11, wherein the shielding film and the gate signal line are tapered~~ around the edge~~.

14. (Original) A digital camera comprising a semiconductor device according to claim 11.

15. (Original) A video camera comprising a semiconductor device according to claim 11.

16. (Original) A goggle type display device comprising a semiconductor device according to claim 11.

17. (Original) An audio system comprising a semiconductor device according to claim 11.

18. (Original) A notebook personal computer comprising a semiconductor device according to claim 11.

19. (Original) A portable information terminal comprising a semiconductor device according to claim 11.

20. (Original) A DVD player comprising a semiconductor device according to claim 11.

21. (Currently Amended) A semiconductor device comprising:

a lower layer capacitance wiring and a gate signal line formed on an insulating surface;

a planarization insulating film formed over the lower layer capacitance wiring and the gate signal line;

a capacitance wiring formed over the planarization insulating film; and

a pixel electrode electrically connected to the capacitance wiring,

wherein the lower layer capacitance wiring overlaps the capacitance wiring with the planarization insulating film sandwiched therebetween~~, and~~

~~wherein the planarization insulating film is polished before the capacitance wiring is formed~~.

22. (Previously Presented) A device according to claim 21, wherein thicknesses of the lower layer capacitance wiring and the gate signal line are 0.1 $\mu$m to 0.5 $\mu$m.

23. (Currently Amended) A device according to claim 21, wherein the lower layer capacitance wiring and the gate signal line are tapered ~~around the edge~~.

24. (Original) A device according to claim 21, wherein the thickness of the planarization insulating film is 0.5 $\mu$m to 1.5 $\mu$m.

25. (Original) A digital camera comprising a semiconductor device according to claim 21.

26. (Original) A video camera comprising a semiconductor device according to claim 21.

27. (Original) A goggle type display device comprising a semiconductor device according to claim 21.

28. (Original) An audio system comprising a semiconductor device according to claim 21.

29. (Original) A notebook personal computer comprising a semiconductor device according to claim 21.

30. (Original) A portable information terminal comprising a semiconductor device according to claim 21.

31. (Original) A DVD player comprising a semiconductor device according to claim 21.

32. (Currently Amended) A semiconductor device comprising:

a shielding film, a lower layer capacitance wiring and a lower layer wiring formed on an insulating surface;

a planarization insulating film formed over the shielding film, the lower layer capacitance wiring and the lower layer wiring;

a thin film transistor including an active layer, the thin film transistor being formed over the planarization insulating film; and

a capacitance wiring formed over the planarization insulating film,

wherein the active layer has a channel formation region,

wherein the shielding film overlaps the channel formation region with the planarization insulating film sandwiched therebetween,

wherein the lower layer capacitance wiring overlaps the capacitance wiring with the planarization insulating film sandwiched therebetween, and

wherein the thin film transistor has a gate electrode electrically connected to the lower layer wiring~~, and~~

~~wherein the planarization insulating film is polished before the active layer is formed~~.

33. (Original) A device according to claim 32, wherein the shielding film, the lower layer capacitance wiring and the lower layer wiring each has a thickness of 0.1 $\mu$m to 0.5 $\mu$m.

34. (Currently Amended) A device according to claim 32, wherein the shielding film, the lower layer capacitance wiring and the lower layer wiring are tapered ~~around their edges~~.

35. (Original) A device according to claim 32, wherein the thickness of the planarization insulating film is 0.5 $\mu$m to 1.5 $\mu$m.

36. (Original) A digital camera comprising a semiconductor device according to claim 32.

37. (Original) A video camera comprising a semiconductor device according to claim 32.

38. (Original) A goggle type display device comprising a semiconductor device according to claim 32.

39. (Original) An audio system comprising a semiconductor device according to claim 32.

40. (Original) A notebook personal computer comprising a semiconductor device according to claim 32.

41. (Original) A portable information terminal comprising a semiconductor device according to claim 32.

42. (Original) A DVD player comprising a semiconductor device according to claim 32.

43. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:

forming a shielding film and a gate signal line over an insulating surface;

forming an insulating film so as to cover the shielding film and the gate signal line;

polishing the insulating film to form a planarization insulating film; and

forming a semiconductor layer having a channel formation region over the planarization insulating film,

wherein the shielding film overlaps the semiconductor layer with the planarization insulating film sandwiched therebetween.

44. (Previously Presented) A method according to claim 43, wherein thicknesses of the shielding film and the gate signal line are 0.1 μm to 0.5 μm.

45. (Currently Amended) A method according to claim 43, wherein the shielding film and the gate signal line are tapered ~~around the edge~~.

46. (Original) A method according to claim 43, wherein the thickness of the planarization insulating film is 0.5 μm to 1.5 μm.

47. (Previously Presented) A method of manufacturing a semiconductor device, comprising the steps of:

forming a shielding film and a gate signal line over an insulating surface;

forming an insulating film so as to cover the shielding film and the gate signal line;

polishing the insulating film to form a planarization insulating film; and

forming a thin film transistor including an active layer over the planarization insulating film,

wherein the active layer has a channel formation region, and

wherein the shielding film overlaps the channel formation region with the planarization insulating film sandwiched therebetween.

48. (Previously Presented) A method according to claim 47, wherein thicknesses of the shielding film and the gate signal line are 0.1 μm to 0.5 μm.

49. (Currently Amended) A method according to claim 47, wherein the shielding film and the gate signal line are tapered ~~around the edge~~.

50. (Original) A method according to claim 47, wherein the thickness of the planarization insulating film is 0.5 μm to 1.5 μm.

51. (Previously Presented) A method of manufacturing a semiconductor device, comprising the steps of:

forming a lower layer capacitance wiring and a gate signal line over an insulating surface;

forming an insulating film over the lower layer capacitance wiring and the gate signal line;

polishing the insulating film to form a planarization insulating film;

forming a capacitance wiring over the planarization insulating film; and

forming a pixel electrode electrically connected to the capacitance wiring,

wherein the lower layer capacitance wiring overlaps the capacitance wiring with the planarization insulating film sandwiched therebetween.

52. (Currently Amended) A method according to claim 51, wherein thicknesses of the lower layer capacitance wiring and the gate signal line are 0.1 μm to 0.5 μm.

53. (Currently Amended) A method according to claim 51, wherein the lower layer capacitance wiring and the gate signal line are tapered ~~around the edge~~.

54. (Original) A method according to claim 51, wherein the thickness of the planarization insulating film is 0.5 μm to 1.5 μm.

55. (Previously Presented) A method of manufacturing a semiconductor device, comprising the steps of:

forming a shielding film, a lower layer capacitance wiring and a lower layer wiring over an insulating surface;

forming an insulating film so as to cover the shielding film, the lower layer capacitance wiring and the lower layer wiring;

polishing the insulating film to form a planarization insulating film; and

forming a capacitance wiring and a thin film transistor that includes an active layer over the planarization insulating film,

wherein the active layer has a channel formation region,

wherein the shielding film overlaps the channel formation region with the planarization insulating film sandwiched therebetween,

wherein the lower layer capacitance wiring overlaps the capacitance wiring with the planarization insulating film sandwiched therebetween, and

wherein the thin film transistor has a gate electrode electrically connected to the lower layer wiring.

56. (Original) A method according to claim 55, wherein the shielding film, the lower layer capacitance wiring and the lower layer wiring each has a thickness of 0.1 $\mu$m to 0.5 $\mu$m.

57. (Currently Amended) A method according to claim 55, wherein the shielding film, the lower layer capacitance wiring and the lower layer wiring are tapered ~~around their edges~~.

58. (Original) A method according to claim 55, wherein the thickness of the planarization insulating film is 0.5 $\mu$m to 1.5 $\mu$m.

59. (Previously Presented) The method of manufacturing a semiconductor device according to claim 43, wherein the semiconductor device is incorporated into an electronic

appliance selected from the group consisting of a video camera, a digital camera, a projector, a head mounted display, a game equipment, a personal computer, a portable telephone, a navigation system, an electronic book, an audio system, a DVD player and a mobile computer.

60. (Previously Presented) The method of manufacturing a semiconductor device according to claim 47, wherein the semiconductor device is incorporated into an electronic appliance selected from the group consisting of a video camera, a digital camera, a projector, a head mounted display, a game equipment, a personal computer, a portable telephone, a navigation system, an electronic book, an audio system, a DVD player and a mobile computer.

61. (Previously Presented) The method of manufacturing a semiconductor device according to claim 51, wherein the semiconductor device is incorporated into an electronic appliance selected from the group consisting of a video camera, a digital camera, a projector, a head mounted display, a game equipment, a personal computer, a portable telephone, a navigation system, an electronic book, an audio system, a DVD player and a mobile computer.

62. (Previously Presented) The method of manufacturing a semiconductor device according to claim 55, wherein the semiconductor device is incorporated into an electronic appliance selected from the group consisting of a video camera, a digital camera, a projector, a head mounted display, a game equipment, a personal computer, a portable telephone, a navigation system, an electronic book, an audio system, a DVD player and a mobile computer.

63. (Currently Amended) The semiconductor device according to claim 1, wherein the planarization film is formed by polishing an insulating film ~~polished~~ by CMP.

64. (Currently Amended) The semiconductor device according to claim 11, wherein the planarization film is formed by polishing an insulating film ~~polished~~ by CMP.

65. (Currently Amended) The semiconductor device according to claim 21, wherein the planarization film is formed by polishing an insulating film ~~polished~~ by CMP.

66. (Currently Amended) The semiconductor device according to claim 32, wherein the planarization film is formed by polishing an insulating film ~~polished~~ by CMP.

67. (Previously Presented) The method of manufacturing a semiconductor device according to claim 43, wherein the insulating film is polished by CMP.

68. (Previously Presented) The method of manufacturing a semiconductor device according to claim 47, wherein the insulating film is polished by CMP.

69. (Previously Presented) The method of manufacturing a semiconductor device according to claim 51, wherein the insulating film is polished by CMP.

70. (Previously Presented) The method of manufacturing a semiconductor device according to claim 55, wherein the insulating film is polished by CMP.

71. (Previously Presented) The semiconductor device according to claim 1, wherein the insulating surface is a surface of a substrate.

72. (Previously Presented) The semiconductor device according to claim 11, wherein the insulating surface is a surface of a substrate.

73. (Previously Presented) The semiconductor device according to claim 21, wherein the insulating surface is a surface of a substrate.

74. (Previously Presented) The semiconductor device according to claim 32, wherein the insulating surface is a surface of a substrate.

75. (Previously Presented) The method of manufacturing a semiconductor device according to claim 43, wherein the insulating surface is a surface of a substrate.

76. (Previously Presented) The method of manufacturing a semiconductor device according to claim 47, wherein the insulating surface is a surface of a substrate.

77. (Previously Presented) The method of manufacturing a semiconductor device according to claim 51, wherein the insulating surface is a surface of a substrate.

78. (Previously Presented) The method of manufacturing a semiconductor device according to claim 55, wherein the insulating surface is a surface of a substrate.

## REMARKS

Claims 1-78 are pending, with claims 1, 11, 21, 32, 43, 47, 51 and 55 being independent. Claims 1, 3, 11, 13, 21, 23, 32, 34, 43, 45, 49, 52, 53, 57 and 63-66 have been amended. No new matter has been introduced.

Applicant acknowledges with appreciation the Examiner's allowance of claims 11-20, 32-46, 55-59, 62, 64, 66, 67, 70, 72, 74, 75 and 78.

Claims 1-10, 21-31, 47-54, 60, 61, 63, 65, 68, 69, 71, 73, 76 and 77 have been rejected as obvious over Morita (U.S. Patent No. 6,259,200) in view of Sato (U.S. Patent No. 6,327,006).

With respect to claim 1 and its dependent claims, applicant requests reconsideration and withdrawal of this rejection because neither Morita, Sato, nor any proper combination of the two describes or suggests a semiconductor layer having a channel formation region formed over the planarization insulating film, as recited in amended claim 1. While the rejection indicates that Morita describes, at col. 4, lines 33-37, an ITO film that constitutes a semiconductor film and is formed over the planarization film, the ITO film does not include a channel formation region. For at least this reason, the rejection should be withdrawn.

With respect to claims 21 and 51, and their dependent claims, applicant requests reconsideration and withdrawal of this rejection because neither Morita, Sato, nor any proper combination of the two describes or suggests a capacitance wiring formed over the planarization insulating film and electrically connected to a pixel electrode, as recited in claims 21 and 51. The rejection asserts that the ITO layer of Morita can be considered to be the top capacitance wiring. However, even assuming for sake of argument that this is the case, neither Morita nor Sato describes or suggests electrically connecting a pixel electrode to the ITO layer, as recited in each of claims 21 and 51. For at least this reason, the rejection should be withdrawn.

With respect to independent claim 47 and its dependent claims 48-50, 60, 68 and 76, applicant requests that the rejection be withdrawn because neither Morita, Sato, nor any proper combination of the two describes or suggests forming a thin film transistor including an active layer over a planarization insulating film, as recited in claim 47. Applicant also notes that the

inclusion of such a thin film transistor has been identified by the Examiner as being the basis for the Examiner's allowance of claims 11-20, 32-46, 55-59, 62, 64, 66, 67, 70, 72, 74, 75 and 78.

Finally, applicant notes that each of claims 1, 11, 21 and 32 has been amended to eliminate the references to polishing the planarization film in view of the Examiner's assertion that the recitation of such polishing is not given patentable weight in device claims.

Applicant submits that all claims are in condition for allowance.

No fee is believed to be due in connection with this paper. In the event that any fees are due, please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

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